

WHAT IS CLAIMED IS:

- 1 1. A circuit for correcting bow in a linear arrangement of
2 elements comprising:
 - 3 a substrate assembly having a plurality of LED elements
 - 4 each having associated driver subassemblies, each of the LED
 - 5 elements representing a pixel within a line;
 - 6 an interface board coupled to the substrate assembly, the
 - 7 interface board having circuitry that processes image data for
 - 8 the LED elements;
 - 9 a course bow correction circuit on the interface board that
 - 10 electronically arranges the pixels to improve linearity by
 - 11 integral numbers of pixel pitch; and
 - 12 a fine bow correction circuit located at least partially on
 - 13 the substrate, the fine bow correction circuit providing a first
 - 14 circuit common to a plurality of the LED elements and a second
 - 15 circuit dedicated to a specific LED element, the second circuit
 - 16 selecting one of a set of a delays that improves linearity of the
 - 17 pixels within the line by a fraction of a pixel pitch.
- 1 2. The circuit of claim 1 wherein the fine bow correction
2 circuit is located entirely on the substrate.
- 1 3. The circuit of claim 1 wherein the fine bow correction
2 circuit is located at least partially on the interface board.
- 1 4. The circuit of claim 3 wherein the fine bow correction
2 circuit that is located at least partially on the interface board provides
3 at least one circuit trace that carries a plurality of signals to the fine
4 bow correction circuit on the substrate, wherein the signals are not
5 concurrently active.

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TABLES 5027860

1 5. The circuit of claim 1 wherein the fine bow correction
2 further comprises:

3 the first circuit providing the set of delays to the plurality
4 of LED elements; and

5 the second circuit selecting one of the delays according to
6 a specific parameter for the LED element.

1 6. The circuit of claim 5 wherein the parameter further
2 comprises a stored value that selects one of delays.

1 7. The circuit of claim 6 wherein the stored value is within
2 the fine bow correction circuit and further comprises at least one
3 multiplexer and at least one latch per LED element.

1 8. The circuit of claim 1 further comprising a delay repeat
2 circuit that creates multiples of the set of delays using the set of
3 delays.

1 9. The printhead of claim 1 wherein the fine bow correction
2 circuit is implemented at a segment level selected from one of the
3 following groups: 2, 4, 8, or 16 LED elements.

1 10. The printhead of claim 1 wherein the interface board
2 further comprises a set of printhead brightness tables and a set of
3 printhead correction tables on the interface board.

1 11. The printhead of claim 1 wherein the LED elements are
2 arranged in a plurality of rows and wherein the second circuit selects
3 different delays for different rows.

1 12. The printhead of claim 11 wherein the plurality of rows
2 further comprises an odd row and an even row, and the second circuit
3 selects delays that are offset by one delay between the odd row and
4 the even.

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1 13. An electronic bow correction method comprising the
2 steps of:

3 providing a linear arrangement of elements on a substrate
4 having an ideal degree of linearity, each of the elements
5 representing pixels having a predetermined pixel pitch and
6 timing means for exposing the elements for a single line time
7 period, the substrate being coupled to an interface board that
8 provides image process electronics for the plurality elements on
9 the substrate;

10 creating a first circuit that places the plurality elements
11 within the single pixel pitch of the ideal degree of linearity;

12 forming a second circuit that comprises a plurality of
13 delays which are each a fraction of the single pixel pitch and
14 means for selecting one of the delays to be applied to the timing
15 means in accordance with a predetermined parameter; and

16 placing the parameter within the means for selecting.

1 14. The method of bow correction within claim 13 wherein
2 the means for selecting further comprises a register and a multiplexer
3 configured to select one of the delays to the timing means in
4 accordance with the predetermined parameter.

1 15. The method of claim 13 wherein the step of forming
2 further comprises forming means for selecting having comprises a
3 software accessible register.

1 16. The method of claim 15 wherein the step of forming
2 further comprises forming the software accessible register such that it
3 can be loaded via a JTAG serial data path.

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1 17. The method of claim 13 wherein the step of forming
2 further comprises forming the second circuit with a delay clock
3 having a fixed clock reference for unique fixed delays which has a
4 frequency that can be changed to produce different delay increments.

1 18. The method of claim 17 wherein the step of forming
2 further comprises the second circuit having a delay repeat function
3 that allows each of the delays to be used multiple times to increase the
4 delays available within a line time.

1 19. The method of claim 13 wherein the step of forming the
2 second circuit further comprises forming the second circuit such that it
3 is located at least partially on the interface board and the part of the
4 second circuit that is formed on the interface board provides at least
5 one circuit trace that carries a plurality of signals to the second circuit
6 portion located on the substrate, wherein the signals are not
7 concurrently active.

1 20. The method of claim 13 wherein the providing step
2 further comprises providing the elements arranged in a plurality of
3 rows and wherein the predetermined parameter selects different delays
4 for different rows.

1 21. The method of claim 20 wherein the plurality of rows
2 further comprises an odd row and an even row, and the predetermined
3 parameter selects delays that are offset by one delay between the odd
4 row and the even row.

1 22. An electronic printing product having pixel alignment
2 circuitry defined by the steps of:

3 providing a substrate having a plurality of printing
4 elements with associated driver circuitry coupled to an interface

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5 board, and timing means for selectively exposing each of the
6 printing elements for a line time;

7 creating a coarse adjustment circuit on the interface
8 board, the coarse adjustment circuit having circuitry that aligns
9 pixel data in integral numbers of line times;

10 forming a fine adjustment circuit located at least partially
11 on the substrate, the fine adjustment circuit providing a
12 plurality of delays to each of the elements, wherein each of the
13 delays is a fraction of an exposure period of the timing means;
14 and

15 selecting one of the delays in accordance with a
16 predetermined parameter.

1 23. The product of claim 22 circuit of claim 16 wherein the
2 step of forming further comprises forming the fine adjustment circuit
3 with a software accessible register for delay selection of each element.

1 24. The product of claim 22 wherein the step of forming
2 further comprises forming the fine adjustment circuit wherein the
3 software accessible register can be loaded via a JTAG serial data path.

1 25. The product of claim 24 wherein the step of forming
2 further comprises forming the fine adjustment circuit wherein a delay
3 clock having a fixed clock reference for unique fixed delays which
4 has a frequency that can be changed to produce different delay
5 increments.

1 26. The product of claim 22 wherein the step of forming
2 further comprises forming the fine adjustment circuit wherein the
3 plurality of delays are modifiable to allow for different levels of fine
4 pixel adjustment.

1 27. The product of claim 22 wherein the step of forming the
2 fine bow correction circuit forms the fine bow correction circuit such
3 that it is located at least partially on the interface board and provides
4 at least one circuit trace that carries a plurality of signals to the fine
5 bow correction circuit on the substrate, wherein the signals are not
6 concurrently active.

1 28. The product of claim 22 wherein the step of selecting
2 further comprises selecting the delays such that the delays are
3 repeated with a first delay following a last delay forming a repeated
4 delay circuit from multiples of the delays.

1 29. The product of claim 22 wherein the step of providing
2 further comprises providing the elements arranged in a plurality of
3 rows and wherein the fine adjustment circuit selects different delays
4 for different rows.

1 30. The product of claim 29 wherein the step of providing
2 further comprises providing as the plurality of rows an odd row and an
3 even row, and the fine adjustment circuit selects delays that are offset
4 by one delay between the odd row and the even row.

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